

## HEAT TREATMENT OF SILICON SEMICONDUCTOR SUBSTRATE

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### Abstract

**PROBLEM TO BE SOLVED:** To carry out predetermined heat treatments efficiently within a short period on a substrate in which oxygen precipitation is hard to grow by forming a non-defect region on the surface layer of a silicon semiconductor substrate, subjecting the resultant to a predetermined high-temperature, short-period heat treatment with rapid heating and cooling, and thereafter subjecting the resultant to a low-temperature, short-period nucleating heat treatment.

**SOLUTION:** A silicon wafer having a predetermined interstitial oxygen concentration of a silicon semiconductor substrate is subjected to a high-temperature heat treatment at 1100 deg.C or higher in a nitrogen diluted oxidative atmosphere for several hours to thereby form a non-defect layer close to the surface of the substrate. Then, the resultant is subjected to a high-temperature heat treatment at 1200 deg.C or higher in an unoxidative atmosphere for 5 to 300 seconds in a heat-treatment furnace capable of both rapidly heating and cooling by increasing and decreasing the temperature at a rate of 10 to 200 deg.C/sec. Then, the resultant is subjected to a low-temperature, short-period nucleation heat treatment at 500 to 900 deg.C. As a result, such minute defects (BMD) as to allow a sufficient intrinsic gettering (IG) effect to be provided inside the silicon semiconductor substrate can be obtained, and the treatment time can also be reduced to a great extent.

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**MACHINE-ASSISTED TRANSLATION (MAT):**

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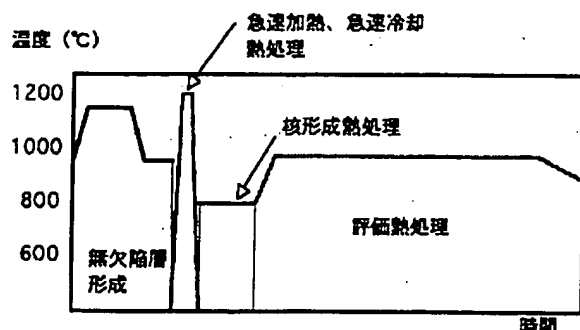
**(57)[SUMMARY]**

**[SUBJECT]** The heat-treatment process of the silicon semiconductor substrate in which a DZ-IG process is possible provides for the substrate on which oxygen deposit seldom grows, efficiently in a short time.

**[SOLUTION]** The oxygen density between lattices of the silicon semiconductor substrate is a  $11 - 17 \times 10^{17}$  (atoms/cm<sup>3</sup>) silicon wafer.

For several hours at high-temperature heat treatment of 1100 degrees C or more within the oxidizing atmosphere of a nitrogen dilution, after making a defect-free layer form near the substrate surface, the heat treating furnace in which rapid heating, such as a lamp annealing reactor, and a quick cooling are possible performs heat treatment of high temperature in a short time within a non-oxidising atmosphere, such as nitrogen and argon.

Compared with a conventional DZ-IG process by performing after that nucleation heat treatment at low temperature in a short time, remarkable shortening of processing time, and quality equivalent to conventional DZ-IG goods is obtained.



[translation of Japanese text in Selection Diagram]

vertical axis: temperature

horizontal axis: time

- 1<sup>st</sup> region: non-defect layer formation
- 2<sup>nd</sup> region: rapid heating, rapid cooling - heat processing
- 3<sup>rd</sup> region: nucleus formation heat processing
- 4<sup>th</sup> region: evaluation heat processing

## [CLAIMS]

**[CLAIM 1]** After heat treatment which makes a defect-free layer form on the outer layer of a silicon semiconductor substrate, at 10-200 degrees C /sec programming rate, within a non-oxidising atmosphere, it raises temperature to 1200 degrees C or more.

After 5 seconds - 300 seconds maintenance at 1200 degrees C - 1300 degrees C, after cooling at a 10-200 degrees C /sec temperature-fall rate, furthermore short-time nucleation heat treatment is performed.

The heat-treatment process of the silicon semiconductor substrate which obtains a substrate with BMD more than  $1 \times 10^8$  (cm<sup>-3</sup>).

**[CLAIM 2]** In Claim 1, the heat-treatment process of a silicon semiconductor substrate with the oxygen density between lattices of the silicon semiconductor substrate  $11 - 17 \times 10^{17}$  (atoms/cm<sup>3</sup>).

**[CLAIM 3]** A heat-treatment process of a silicon semiconductor substrate the specific resistance of a silicon semiconductor substrate is 0.001 - 100((OMEGA)cm) in Claim 1.

**[CLAIM 4]** In Claim 1, for nucleation heat treatment in an oxidizing atmosphere, the heat-treatment process of the silicon semiconductor substrate which is a process maintained for 0.5 to 30 hours in the 500 - 900 degree C temperature range.

**[CLAIM 5]** Heat treatment which makes a defect-free layer form in Claim 1 is the heat-treatment process of the silicon semiconductor substrate which is a process maintained for 0.5 to 30 hours above 1100 degrees C.

### **[DETAILED DESCRIPTION OF INVENTION]**

#### **[0001]**

**[TECHNICAL FIELD]** This invention concerns improvement of the DZ-IG heat-treatment process of a silicon semiconductor substrate.

After making a defect-free layer form on the outer layer of the substrate, by rapid heating and a quick cooling within a non-oxidising atmosphere, high temperature and short-time heat treatment is performed.

Nucleation heat treatment of low temperature in a short time is performed after that, and it is related with the heat-treatment process of the silicon semiconductor substrate which makes the inside of the substrate precipitate efficiently the micro defect of a grade which can anticipate IG effect.

#### **[0002]**

**[PRIOR ART]** As the process of receiving thing metal-impurity in a semiconductor substrate in the manufacturing process, intrinsic Gettering (it describes as IG henceforth) method is known.

This is a method of utilizing the described micro defect (Bulk Micro Defect in a silicon semiconductor substrate, BMD henceforth).

**[0003]** Moreover, in order to apply a silicon semiconductor substrate to a device process, high-temperature heat treatment of 1100 degrees C or more is beforehand performed within an oxidizing atmosphere.

After forming the defective layer without diffusing outward oxygen between

outer-layer lattices of the silicon semiconductor substrate, it describes as DZ layer (Denuded Zone, henceforth).

BMD is made to form on the inside of the silicon semiconductor substrate by a low-temperature process, and IG-effect needs to be given.

This series of heat treatment is called the "DZ-IG process".

**[0004]** However, since the amount of precipitation of BMD changes with the oxygen densities between the lattices and the specific resistances of a silicon semiconductor substrate about above-mentioned IG process, various IG process heat sequences are utilized.

When antimony (in the following, Sb ) is especially used as a dopant of the silicon semiconductor substrate, specific resistance is about 0.001 - 0.1(( $\Omega$ cm), there is a characteristic that oxygen deposits very seldom grow.

Therefore a long time is required for precipitation heat treatment, and there is a problem in the viewpoint of productivity.

**[0005]**

**[PROBLEM ADDRESSED]** In the above-mentioned DZ-IG process, the oxygen density between lattices of the silicon semiconductor substrate is  $11 - 17 \times 10^{17}$ (atoms/cm<sup>3</sup>) silicon wafer.

Several hours are performed a high-temperature process at 1100 degrees C or more within the oxidizing atmosphere of the nitrogen dilution.

After making a defect-free layer form near the substrate surface, heat treatment for making BMD form on the inside of the substrate is used.

**[0006]** For example, after a high-temperature process maintained at 1150 degrees C as shown in diagram 7, the method for fixed-temperature heat treatment by several-dozens-of-hours maintenance in the 500 - 600 degree C temperature range, after a high-temperature process maintained at 1150 degrees C as shown in diagram 8, a silicon semiconductor substrate is supplied to a heat treating furnace by the 500 - 600 degree C temperature range.

There is a process of increasing temperature to 800-900 degrees C after that.

**[0007]** As The necessary time for IG process for securing BMD density, i.e.,

1\*10<sup>8</sup> - 1\*10<sup>10</sup>(cm<sup>-3</sup>), and size of a required level for gettering by the above-mentioned heat-treatment process, the oxygen density between the lattices and the specific resistance of a silicon semiconductor substrate are decided, and the heat-treatment time is about 10-100 hours.

About the heat treatment which needs a long time also, productivity is very bad.

**[0008]** On the other hand, for example, a silicon semiconductor substrate is heated at a high-temperature (1100 - 1280 degree C). After thermal equilibrium concentration of point defects making the point defect exist, by carrying out rapid cooling to 500 degrees C or less with the cooling rate greater than 200 degree-C /min, and making supersaturation, there is a method of obtaining BMD required for a gettering in a short time (Japanese-Patent-Publication-gazette No. 3-9078).

However, surely, by the above-mentioned heat-treatment process, high density BMD is obtained with short-time heat treatment.

However, BMD grows also near the silicon semiconductor-substrate surface, and the problem which degrades quality of the device barrier layer is generated.

**[0009]** The specific resistance in which this invention has the characteristic that oxygen deposits very seldom grow, for example, by which Sb dope was carried out makes the defect-free layer form on the outer layer of the substrate 0.001 - 0.1((OMEGA)cm) silicon semiconductor substrate.

And the inside of a substrate is made to precipitate the micro defect of a grade which can anticipate IG effect.

Namely, it aims at the offer of the heat-treatment process of the silicon semiconductor substrate in which a DZ-IG process is possible on the substrate for which oxygen deposit seldom grows, efficiently in a short time.

**[0010]**

**[SOLUTION OF THE INVENTION]** Inventors did various examination for the purpose of the heat-treatment process which enables a DZ-IG process in a short time efficiently on the substrate on which oxygen deposit seldom grows.

As a result, the oxygen density between lattices of the silicon semiconductor substrate is 11 - 17\*10<sup>17</sup>(atoms/cm<sup>3</sup>) silicon wafer.

For several hours at high-temperature heat treatment of 1100 degrees C or more within the oxidizing atmosphere of a nitrogen dilution, after making a defect-free layer form near the substrate surface, the heat treating furnace in which rapid heating, such as a lamp annealing reactor, and a quick cooling are possible performs heat treatment of high temperature in a short time within a non-oxidising atmosphere, such as nitrogen and argon.

Compared with a conventional DZ-IG process by performing after that nucleation heat treatment at low temperature in a short time, equivalent quality, with remarkable shortening of processing time compared with conventional DZ-IG goods is obtained, and this is known.

This invention was perfected.

**[0011]** This invention, after heat treatment which makes the defect-free layer form on the outer layer of a silicon semiconductor substrate, or succeedingly, it raises temperature within non-oxidising atmosphere to above-mentioned heat treatment, and it raises temperature to 1200 degrees C or more by 10-200 degrees C / sec programming rate.

It cools by 10-200 degrees C / sec in temperature-fall speed after 5 seconds - 300 second maintenance at 1200 degrees C - 1300 degrees C.

Furthermore, nucleation heat treatment maintained for 0.5 to 30 hours in the 500 - 900 degree C temperature range is performed.

It is the heat-treatment process of the silicon semiconductor substrate which obtains a substrate BMD more than  $1 \times 10^8$  (cm<sup>-3</sup>).

**[0012]**

**[Embodiment]** In this invention, the oxygen density between lattices of the silicon semiconductor substrate is  $11 - 17 \times 10^{17}$  (atoms/cm<sup>3</sup>) silicon wafer. for several hours are performed high-temperature heat treatment of 1100 degrees C or more within the oxidizing atmosphere of nitrogen dilution.

After making a defect-free layer form near the substrate surface, in the heat treating furnace in which rapid heating, such as a lamp annealing reactor, and a quick cooling are possible, high-temperature heat treatment of 1200 degrees C or more is performed for 5-300 seconds by 10-200 degrees C / sec in rising-and-falling-temperature speed, within non-oxidising atmosphere, BMD of a grade which can anticipate sufficient IG effect inside the silicon semiconductor



substrate is obtained by performing after that nucleation heat treatment of 500-900-degree C low temperature in a short time, and processing time can also be shortened remarkably.

**[0013]** For the target silicon semiconductor substrate in this invention, the oxygen density between lattices of the substrate is  $11 - 17 \times 10^{17}$  atoms/cm<sup>3</sup>, and the specific resistance is 0.001 - 100(OMEGA)cm.

Preferably it is the silicon semiconductor substrate by which Sb dope was carried out, and the specific resistance is 0.001 - 0.1(OMEGA)cm.

It is aimed at the range of previous specific-resistance values for oxygen deposits very seldom growing.

Moreover, BMD density will be set to  $1 \times 10^8$  (cm<sup>-3</sup>) if the initial oxygen density is outside  $11 - 17 \times 10^{17}$  atoms/cm<sup>3</sup> ranges, and the gettering efficiency becomes weak.

Moreover, at BMD density more than  $1 \times 10^8$  (cm<sup>-3</sup>), the mechanical strength of the silicon semiconductor substrate may become weak.

**[0014]** Below, the heat-treatment process of this invention is demonstrated based on the heat pattern diagram of diagram 1.

As for heat treatment which makes the defect-free layer of the first stage form, in this invention, it is good to perform a high-temperature process of 1100 degrees C or more for several hours within the oxidizing atmosphere of nitrogen dilution.

At temperature lower than 1100 degrees C, since the outside diffusion of oxygen is slow, a extended process is required.

Moreover, what also has the sufficient quality of a defect-free layer is not obtained.

Therefore, the temperature of 1100 degrees C or more is required.

Preferably, it is a process maintained for 2 to 5 hours at 1100 degrees C - 1150 degrees C.

**[0015]** After heat treatment of the rapid heating which is the characteristic in the heat-treatment process of this invention, and a quick cooling finalized heat treatment which makes the defect-free layer of the first stage form, and also it is moved to a non-oxidising atmosphere and undergoes a rapid heating from about 25 degrees C. during the first stage cooling, for example, it may start from

about 600 degrees C.

Moreover, a heat-treatment process is raised temperature at 1200 degrees C or more by 10-200 degrees C / sec programming rate within non-oxidising atmosphere.

After 5 seconds - 300 second maintenance to 1200 degrees C - 1300 degrees C, at 10-200 degrees C / sec temperature-fall speed, it cools to about room-temperature - 900 degrees C.

**[0016]** Moreover, as a rapid heating and heat-treatment conditions of quick cooling, the programming rate and the temperature-fall speed are under 10 degree-C / seconds.

Or when less than 5 seconds heat treatment is performed at less than 1200 degrees C, IG effect for it that the amount of precipitation of BMD is low in the inside of a silicon semiconductor substrate, and is sufficient is not obtained. The programming rate and the temperature-fall speed exceed 200 degree-C / second.

The heat-treatment time exceeds 300 seconds.

Since there is a problem which silicon semiconductor-substrate slip transition generates when heat treatment is performed at the temperature exceeding 1300 degrees C, it is considered as the above-mentioned range.

**[0017]** In this invention, in order not to make the endurance of the lamp which is the heat source of a lamp annealing reactor reduce, related with a heat-treatment time, since there is no remarkable variation in the amount of precipitation of BMD in 60 seconds or more, it raises temperature by 10-100 degrees C / sec programming rate.

After 5 seconds - 60 second maintenance to 1200 degrees C - 1250 degrees C, the process cooled to about 600 degrees C by 50-100 degrees C / sec in temperature-fall speed is especially preferable.

**[0018]** As nucleation heat treatment which is next as the 3rd stage of the heat-treatment process in this invention, it is less than 500 degrees C.

When 900 degrees C was exceeded and a short-time fixed-temperature maintenance process is performed, since IG effect for it that the amount of precipitation of BMD is low inside of a silicon semiconductor substrate, and is sufficient is not obtained, as nucleation heat-treatment temperature, inside the

500 degrees C - 900 degrees C temperature range, it is desirable to perform at 700 degrees C - 800 degrees C especially.

Moreover as the holding time, 3-5 hours is desirable.

Any of inert atmospheres, such as argon gas, an oxidizing atmosphere, nitrogen atmosphere, or its mixed-gas atmosphere are sufficient as the atmosphere.

#### [0019]

##### [Embodiment]

##### Embodiment 1

As for the growth by the CZ process, the surface bearing was (100), the oxygen density between lattices is  $15 \times 10^{17}$  (atoms/cm<sup>3</sup>). The specific resistance in the silicon wafer of 200 mm outer diameter is more than one (OMEGA) (cm). The heat pattern as shown in diagram 1 was heat-treated.

First, heat treatment of 3.5 hours is performed in 3% oxygen containing N<sub>2</sub> atmosphere at 1150 degrees C.

The defect-free layer was made to form on the wafer outer layer.

[0020] Next, with the above-mentioned wafer within nitrogen atmosphere in the lamp annealing reactor. After maintaining for 60 seconds after raising temperature to 1150 - 1300 degree C various temperature by the 50 degrees-C / second programming rate, heat treatment cooled by the 50 degrees-C / second in temperature-fall speed was performed.

Then, after performing nucleation heat treatment which maintains the above-mentioned wafer for 5 hours at 800 degrees C within oxygen atmosphere, 1000 degrees C and the precipitation heat treatment of a 16 hour retaining were performed.

[0021] In order to observe BMD inside the silicon wafer, 2 micrometre etching is given on the cross section of a silicon wafer by the light etching solution.

The cross section was counted as an etch pit by the light microscope.

The result is shown in diagram 2.

The compounding ratios of the light etching solution at this time was as follows.

HF:HNO<sub>3</sub>:CrO<sub>3</sub>:Cu(NO<sub>3</sub>)<sub>2</sub>:H<sub>2</sub>O:CH<sub>3</sub>COOH=60cc:30cc:30cc:2g:60cc:60cc

(Refer to Applied physics, 45,1055(1976) Takano, Yukio, and Maki, Michiyoshi)

**[0022]** In order to obtain BMD which is the grade which can anticipate IG effect in the silicon substrate from diagram 2, 1200 degrees C or more is required as the lamp annealing process temperature.

It turns out that BMD density at that time is  $1 \times 10^8 - 1 \times 10^9$  (cm<sup>-3</sup>).

Moreover the silicon-substrate cross section at that time has the structure which is shown in diagram 3.

The range of the depth from the surface to about 100 micrometres was the defect-free layer.

**[0023]** Moreover, it evaluated about the silicon wafer which does not perform a lamp annealing process, for comparison.

As a result, it was  $3 \times 10^7$  (cm<sup>-3</sup>), and it was confirmed that precipitation of BMD was low.

Furthermore, about the silicon wafer which carried out the rapid-heating process at 1300 degrees C, there is no remarkable variation of BMD and slip transition had generated from the support part of the silicon wafer.

#### **[0024]** Embodiment 2

The surface bearing (100) by the growth was carried out by the CZ process, and the oxygen density between lattices is  $15 \times 10^{17}$  (atoms/cm<sup>3</sup>). The specific resistance in the silicon wafer of 200 mm outer diameter is more than one (OMEGA) (cm). Heat treatment of 3.5 hours is performed in 3% oxygen containing N<sub>2</sub> atmosphere at 1150 degrees C.

The defect-free layer was made to form on the wafer outer layer.

**[0025]** For the above-mentioned wafer within nitrogen atmosphere in the lamp annealing reactor, it is a 50 degrees-C / second programming rate, and it is 1150 degrees C. After raising temperature variously to 1200 degrees C, 1250 degrees C, and 1300 degrees C, after maintaining for 5 seconds, 60 seconds, 120 seconds, and 300 seconds, heat treatment cooled by the 50 degrees-C / second in temperature-fall speed was performed.

Then, after performing nucleation heat treatment which maintains the above-mentioned wafer for 5 hours at 800 degrees C within oxygen atmosphere, 1000 degrees C and the precipitation heat treatment for 16 hour retaining was

performed.

Subsequently the result which observed BMD like embodiment 1 is shown in diagram 4.

**[0026]** It is the wafer which, on the one hand, made the above-mentioned defect-free layer form, within nitrogen atmosphere in a lamp annealing reactor.

With a programming-rate of 10,50,100,200 degree-C / second, after raising temperature variously to 1150 degrees C, 1200 degrees C, 1250 degrees C, and 1300 degrees C, after maintaining for 60 seconds, heat treatment cooled by the temperature-fall speed 10,50,100,200 degree-C / second was performed.

Then, after performing nucleation heat treatment which maintains the above-mentioned wafer for 5 hours at 800 degrees C within oxygen atmosphere, 1000 degrees C and the precipitation heat treatment for 16 hour retaining was performed.

Subsequently the result which observed BMD like embodiment 1 is shown in diagram 5.

**[0027]** Heat-treatment temperature is 1200 degrees C or more as a rapid heating and quick-cooling process conditions from diagram 4 and diagram 5.

And with 5 seconds or more as the heat-treatment time,  $1 \times 10^8 - 2 \times 10^9 (\text{cm}^{-3})$  BMD is obtained inside the silicon substrate. It was confirmed that sufficient IG effect was expectable.

Moreover, the remarkable variation of BMD was not seen using heat-treatment time for 60 seconds or more.

**[0028]** Moreover, also about rising-and-falling-temperature speed, when it was more than the 10 degree-C / second,  $1 \times 10^8 - 3 \times 10^9 (\text{cm}^{-3})$  BMD was obtained.

However, there is no remarkable variation of BMD about the rising-and-falling-temperature speed more than a 100 degree-C / second, and slip transition had occurred in the silicon semiconductor substrate.

### **[0029] Embodiment 3**

In embodiment 1, the specific resistance using Sb as a dopant of a silicon semiconductor substrate is  $0.005 ((\Omega \text{cm}))$  silicon wafer.

Heat treatment of 3.5 hours is performed in 3% oxygen containing N<sub>2</sub> atmosphere and 1150 degrees C.

After making a defect-free layer form near the wafer surface, after maintaining the above-mentioned wafer for 60 seconds after raising temperature in various temperature of 1150 degrees C, 1200 degrees C, 1250 degrees C, and 1300 degrees C by the 50 degrees-C / second programming rate within nitrogen atmosphere in a lamp annealing reactor, heat treatment cooling at 50 degrees-C / second in temperature-fall speed was performed.

Then, after performing nucleation heat treatment which maintains the above-mentioned wafer for 10 hours at 800 degrees C within oxygen atmosphere, the precipitation heat treatment of retaining was performed for 16 hours at 1000 degrees C.

Subsequently the result which observed BMD like embodiment 1 is shown in diagram 6.

**[0030]** Clearly from diagram 6, if it is 1200 degrees C or more as the rapid heating and quick-cooling heat-treatment temperature,  $1 \times 10^8 - 1 \times 10^9 (\text{cm}^{-3})$  BMD is obtained inside the silicon substrate, and it was confirmed that sufficient IG effect is expectable.

However, by 1300-degree C heat treatment, it was confirmed like the above-mentioned embodiment 1 that there is no remarkable variation of BMD and slip transition has occurred in the silicon semiconductor substrate.

In addition, it was evaluated also about that which does not perform the above-mentioned lamp annealing process as an object for comparison.

As a result, it becomes below  $1 \times 10^6 (\text{cm}^{-3})$ , and practically no BMD was obtained.

#### **[0031]**

**[EFFECT OF THE INVENTION]** This invention performs the high temperature of a rapid heating and a quick cooling, and short-time heat treatment, after making a defect-free layer form on the outer layer of a silicon semiconductor substrate.

BMD of the grade which can anticipate IG effect inside the silicon semiconductor substrate like conventional DZIG process in a short time can be obtained by performing after that nucleation heat treatment at low temperature in a short time.

Productivity is high for the quality silicon semiconductor substrate.

It can be provided stably.

**[BRIEF EXPLANATION OF DRAWINGS]**

**[FIGURE 1]** The graph which shows the heat pattern of the heat-treatment process by this invention.

**[FIGURE 2]** The heat-treatment temperature dependency of the heat-treatment process by this invention is shown. It is the graph of BMD density after heat treatment.

**[FIGURE 3]** The cross-sectional explanatory drawing of the silicon wafer after heat treatment by this invention.

**[FIGURE 4]** The heat-treatment temperature dependency of the heat-treatment process by this invention is shown. It is the graph of BMD density after heat treatment.

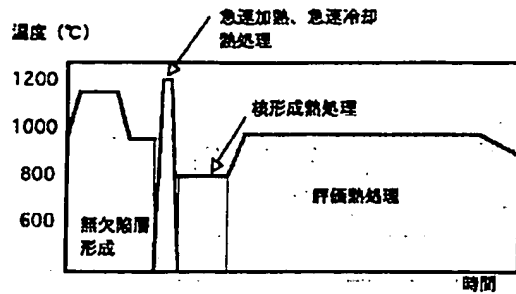
**[FIGURE 5]** The graph of BMD density after heat treatment which shows the rising-and-falling-temperature speed dependence of the heat-treatment process by this invention.

**[FIGURE 6]** The graph of BMD density after heat treatment which shows the other heat-treatment temperature dependency of the heat-treatment process by this invention.

**[FIGURE 7]** The graph which shows the heat pattern of conventional DZ-IG processing method.

**[FIGURE 8]** The graph which shows the other heat pattern of conventional DZ-IG processing method.

**[FIGURE 1]**



[translation of Japanese text in Figure 1]

vertical axis: temperature

horizontal axis: time

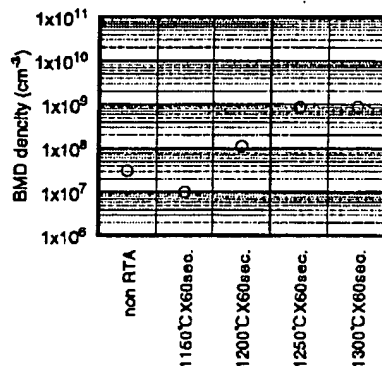
1<sup>st</sup> region: non-defect layer formation

2<sup>nd</sup> region: rapid heating, rapid cooling - heat processing

3<sup>rd</sup> region: nucleus formation heat processing

4<sup>th</sup> region: evaluation heat processing

[FIGURE 2]



[FIGURE 3]

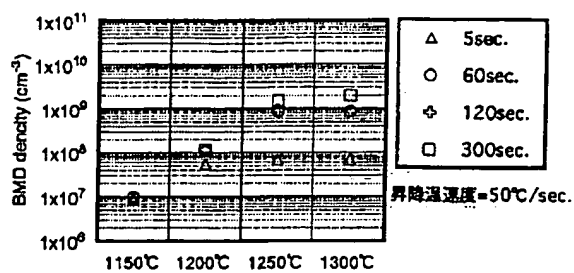


[translation of Japanese text in Figure 3]

non-defect layer surface - approx. 100μm

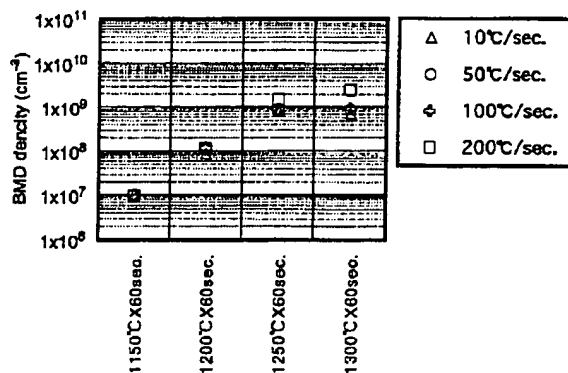
[FIGURE 4]



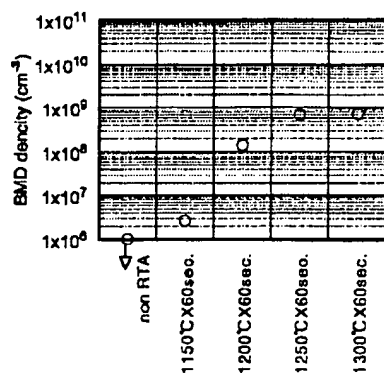


[translation of Japanese text in Figure 4]  
rate of temperature rise

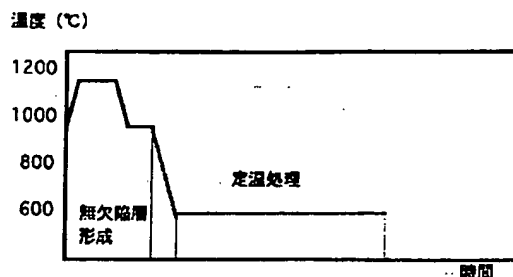
[FIGURE 5]



[FIGURE 6]



[FIGURE 7]



[translation of Japanese text in Figure 7]

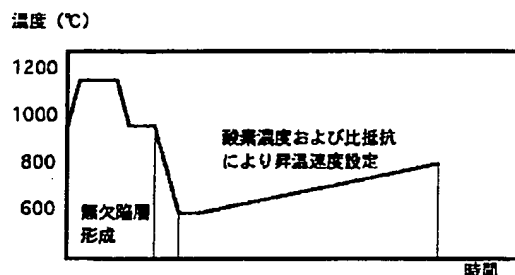
vertical axis: temperature

horizontal axis: time

1<sup>st</sup> region: non-defect layer formation

2<sup>nd</sup> region: steady temperature processing

[FIGURE 8]



[translation of Japanese text in Figure 8]

vertical axis: temperature

horizontal axis: time

1<sup>st</sup> region: non-defect layer formation

2<sup>nd</sup> region: setting of temperature rise rate depending on oxygen concentration and specific resistance

# [AMENDMENTS]

[Filing date] May 1st, Heisei 10

[Am ndm nt 1]

**[Title of document for amendment]** Description

**[Item to be amended]** 0031

**[Method of amendment]** Alteration

**[Content of amendment]**

**[0031]**

**[EFFECT OF THE INVENTION]** This invention performs the high temperature of a rapid heating and a quick cooling, and short-time heat treatment, after making a defect-free layer form on the outer layer of a silicon semiconductor substrate.

BMD of the grade which can anticipate IG effect inside the silicon semiconductor substrate like conventional DZ-IG process in a short time can be obtained by performing after that nucleation heat treatment of low temperature in a short time. Productivity is high for the quality silicon semiconductor substrate, and it can be provided stably.

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